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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,802	07/15/2003	Jason P. Brenden	V44.12-0155	7682

164 7590 08/16/2005

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,802	BRENDEN, JASON P.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9* is/are allowed.

6)☒ Claim(s) *10,11,13,22 and 23* is/are rejected.

7)☒ Claim(s) *14-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The appeal brief filed on 6/27/05 has been received and entered in the case. In view of the arguments presented therein, the previous rejections based on Sziebert and Skelton are now withdrawn. In view of newly discovered prior art, however, new rejections are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted.

2. The drawings are objected to because Fig. 1 needs a "prior art" label. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. Claims 10,11, 13, 22 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation of the "feedback networks" being coupled to the first and second input signal nodes is incorrect because, as shown in instant Fig. 2, there is no first feedback network coupled to both the first and second signal input nodes VIP and VIN (because the resistors R1 through R3 are not part of any feedback circuitry, and it is thus improper to refer to them as such). The same is true for the claimed limitation of the second feedback network being coupled to both the first and second signal input nodes.

4. Claims 10, 13, 22 and 23, to the extent understood in light of the above-noted 112 rejection, are rejected under 35 U.S.C. 102(b) as being anticipated by O'Farrell.

Note Figs. 1 and 2, where the recited "first input node" reads on the output terminal of control circuit 50 that is coupled to the inverting input of amplifier 40 through the unnumbered resistor; the recited "second input node" reads on the terminal receiving VREF (i.e., the terminal coupled to the non-inverting input of amplifier 40 through another unnumbered resistor; the recited "first and second VCM nodes" read on nodes 46 and 48, respectively; the recited first through fourth transistors read on FETs 30, 32, 34 and 36, respectively; the recited first power amplifier circuit reads on the combination of op amp 40 and the associated resistors coupled to its input and output terminals (the first feedback network); the recited second power amplifier circuit reads on the combination of op amp 42 and the associated resistors coupled to its input and output terminals (the second feedback network).

5. Claims 10, 11, 22 and 23, to the extent understood in light of the above-noted 112 rejection, are rejected under 35 U.S.C. 102(b) as also being anticipated by Salina et al.

Note Fig. 3, where the recited "first input node" reads on the (+) input of the single op amp of POWER OPAMP PLUS; the recited "second input node" reads on the terminal receiving VCV2; the recited first and second single operational amplifiers are illustrated within POWER OPAMP PLUS and POWER OPAMP MINUS; the recited "first and second VCM nodes" read on nodes VC+ and VC-, respectively; the recited first through fourth transistors read on the four NDMOS transistors Md1 through Md4. The first and second feedback networks are from the nodes across R_SENSE back to the first and second op amps through SENSE AMPLIFIER G, the circuit ERROR AMPLIFIER, PWM CONVERTER, etc.

6. Claims 10, 13, 22 and 23, to the extent understood in light of the above-noted 112 rejection, are also rejected under 35 U.S.C. 102(b) as being anticipated by Chappran et al.

Note Fig. 4, where the recited "first input node" reads on the IN+ of the single op amp OP1 (on the right

side of the figure); the recited "second input node" reads on the terminal receiving IN- (on the right side of the figure); the recited first and second single operational amplifiers are OP1, OP1 (on opposite sides of the figure; the recited first through fourth transistors read on the four NDMOS transistors M4, M3 (two opposing pairs). The first and second feedback networks are from the nodes Vo across the load back to the first and second op amps through resistors R1 (note that both feedback networks are coupled (directly or indirectly) to the first and second input signal nodes.

7. Claims 10, 11, 13, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinozaki.

Note Fig. 1, where the first and second input nodes are where IN and VR are received; the first through fourth transistors are P32, P31, N32 and N31, respectively; the op amps are A61 and A51; and the feedback networks are from output nodes O1 and O2 back to the op amps.

Not disclosed is a second input terminal connected to both feedback networks but such would have been obvious to the ordinarily skilled artisan who will easily recognize the benefit of a single input node for receiving voltage VR

(rather than two separate node for receiving this voltage (the motivation being to simplify the circuit). Also obvious is the use of one or more resistors in the feedback networks (claim 13), as noted above.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salina et al.

The insertion of one or more resistors in the first and second feedback paths (or internally within the single op amps of Salina et al would have been obvious to those having ordinary skill in the art because such feedback resistors are old and well-known in the art for achieving certain benefits/advantages (e.g., to change the circuit operation/gain).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Farrell or Chappran et al.

The use of NDMOS transistors for implementing the first through fourth FETs 30, 32, 34 and 36, though not disclosed, nevertheless would have been obvious to those having ordinary skill in the art who know that these well-known transistors have certain benefits not achieved by ordinary MOSFETs, thus providing the motivation to use

NDMOS transistors (also note the use of these types of FETs in Salina et al).

10. Claims 10, 11, 13, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinozaki.

Note Fig. 1, where the first and second input nodes are where IN and VR are received; the first through fourth transistors are P32, P31, N32 and N31, respectively; the op amps are A61 and A51; and the feedback networks are from output nodes O1 and O2 back to the op amps.

Not disclosed is a second input terminal connected to both feedback networks but such would have been obvious to the ordinarily skilled artisan who will easily recognize the benefit of a single input node for receiving voltage VR (rather than two separate node for receving this voltage (the motivation being to simplify the circuit). Also obvious is the use of one or more resistors in the feedback networks (claim 13), and the use of NDMOS transistors (claim 11) for forming the first through fourth transistors, as noted above.

11. Claims 1-9 are allowed.

Claims 14-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. In view of the above-noted new grounds of rejection, this office action is non-final.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

August 4, 2005